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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, JULY 2017

Course Code: EC206

Course Name: COMPUTER ORGANISATION (EC)

Max. Marks: 100 Duration: 3 Hours

PART A

Question No.1 is compulsory. Answer question 2 or 3. Each carries 15 marks.

1 a) Design a multiplier to multiply two 4-bit numbers. Illustrate with an example. (8)

b) Convert the following MIPS assembly code into machine language. Write the instructions in hexadecimal. (7)

```
addi $s0, $0, 73
sw $t1, -7($t2)
sub $t1, $s7, $s2
```

2 a) Design a shifter that always shifts a 32 bit input left by 2 bits. The input and output are both 32 bits. Explain the design and sketch a schematic. (6)

b) Show the schematic of a sign extension unit with a 4-bit input and an 8-bit output. (4)

c) Express the following base 10 numbers in IEEE 754 single precision floating-point format: (5)

(i) -13.5625 (ii) 42.3125

OR

3 a) Differentiate Big-Endian and Little-Endian machines. (3)

b) Explain the various instruction formats of MIPS with examples. (7)

c) Give a brief account of the architecture of MIPS. (5)

PART B

Question No.4 is compulsory. Answer question 5 or 6. Each carries 15 marks.

4 a) Explain any three state elements of a MIPS processor. (5)

b) What is an exception? How exceptions are classified and handled? (7)

c) Mention any three advantages of multi cycle implementation compared to single cycle implementation. (3)

5 a) Explain various addressing modes of MIPS with examples. (10)

b) What is the range of instruction addresses to which conditional branches such as **beq** and **bne** can branch in MIPS? Give your answer in number of instructions relative to the conditional branch instructions. (5)

OR

6 a) Draw the data path for single cycle processor for R-type instruction along with the control signals. Explain the design procedure for the control unit. (9)

b) Draw the datapath for multicycle processor for R-type instruction and explain (6)

PART C

Question No.7 is compulsory. Answer question 8 or 9. Each carries 20 marks.

7 a) Briefly explain the standard I/O interfaces:- (10)
(i) Serial port (ii) Parallel port (iii) USB.

b) Explain clearly the address translation mechanism in virtual memory. (10)

8 a) Draw the internal organization of a SRAM cell and explain the read and write operation. (10)

b) Explain DMA data transfer method. What are the advantages of DMA transfer? (10)

OR

9 a) Explain direct mapped cache structure. (8)

b) Here is a series of address references given as word addresses: (12)
1,4,8,5,20,17,19,56,9,11,4,43,5,6,9,17.
Assuming a direct mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the final contents of the cache.

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